19.3 A Digital Input Controller for Audio Class-D Amplifiers with 100W 0.004% THD+N and 113dB DR

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An analog-input closed-loop topology for audio class-D amplifiers has the potential of achieving very high audio performance because it can be designed with feedback from the power stage. Other approaches utilizing closed-loop topologies [1, 2] have achieved around 0.01% THD+N, and a class-D amplifier using a pulse-density modulation (PDM) switching scheme [3] has reported good performance with 0.00384% THD+N, 1W output power and 103dB DR. However, PDM switching has one drawback in comparison with PWM. The wide-band spread spectrum and tones of the PDM switching interfere with AM/FM radio signals, while the PWM switching scheme is able to control the carrier frequency to avoid such interference. These topologies also require a DAC and an anti-aliasing filter at the front of the amplifier for use with digital audio sources. A class-D amplifier with integrated DAC [4] which has digital input capability and feedback from the power stage, but uses PDM switching to achieve a direct connection between the DAC and the feedback loop, achieved 83dB DR and 0.1% THD+N with 1W output power.

This paper presents a new controller architecture for audio class-D amplifiers using a PWM switching scheme with a digital input provided by an integrated DAC, which has a special configuration to realize direct connection between the DAC and the feedback loop. Very high audio performance is achieved; 0.0018% THD+N at 10W output power, 0.004% THD+N with 100W output power and 113dB dynamic range.

Figure 19.3.1 shows the controller block diagram consisting of a digital volume circuit, an over-sampling digital filter, a delta-sigma modulator, a current-segmented signal DAC and a pulse-width modulator with loop filter and power stage feedback. After the digital volume, the input digital signal is over sampled, noise-shaped and re-quantized through the digital filter and the delta-sigma modulator. The noise-shaped signal is converted into a current-mode signal in the current-segmented signal DAC, and drives the loop filter of the pulse-width modulator directly. The output of the loop filter is converted to a PWM signal by comparing it to a triangle wave. This two-level class-AD PWM output drives the power stage which is connected to the loop filter feedback through a resistor attenuator.

Generating the PWM by comparing the signal to a triangle wave causes aliasing components if the input has high-frequency components close to twice the carrier frequency of the PWM [5]. This aliasing problem can be avoided by proper synchronization between the signal DAC and the triangle carrier used. A beneficial synchronization having minimum aliasing is achieved when the DAC operates at a sampling frequency exactly twice the PWM frequency. In that case, the noise shaper removes noise from all the critical aliasing bands at multiples of twice the PWM frequency. A direct PW modulation of such a synchronized DAC output signal is identical to an asymmetrical uniform sampling PWM (UPWM) process, which produces an unacceptable amount of harmonic distortion. However, this problem can be solved by proper design of the feedback loop. The PWM feedback loop can be characterized by its signal- and noise-transfer functions, STF and NTF. The NTF of the feedback loop is designed to suppress distortion from the power stage switching. The STF of the loop constitutes the reconstruction filter for the DAC. By proper design, this mechanism can modify the resulting PWM process from a nonlinear UPWM to the highly linear natural sampling PWM (NSPWM).

A Block diagram of the loop filter is shown at the top of Fig. 19.3.2. The 3rd-order distributed feedback configuration of the loop filter realizes a 3rd-order high-pass filter characteristic for the NTF to suppress distortion from the power stage, and a 3rd-order low-pass filter characteristic for the STF to reconstruct the DAC output, thus achieving a near perfect NSPWM process at the comparator input. The triangle wave used for the PWM is generated by injecting a square wave into the input of the 3rd-stage integrator. This square wave injection provides the triangle wave superimposed at the output of the 3rd-stage integrator. The exact circuit implementation of the loop filter is shown at the bottom of Fig. 19.3.2. The current-mode output of the DAC is directly connected to the 1st-stage integrator. Another smaller size current-segmented DAC, called the clock DAC, is used to inject the square wave into the 3rd-stage integrator for the triangle wave superimposition. The input data for the clock DAC is the input clock divided by 2, which also triggers the DAC sampling. Thus, the output of the clock DAC is square wave at half the DAC sampling frequency. All circuits are implemented in fully differential circuits for good noise immunity.

The THD+N is plotted versus output power in Fig. 19.3.3; the input frequency is 1kHz and the results are plotted for R_L = 4, 6, and 8Ω. All the plots have the same shape, the only difference is the shift of output power. Therefore, the THD+N performance is not dependent on the output power and the power-stage characteristic. All distortion from the power stage is suppressed by the feedback, and the output THD+N performance only depends on the input level into the controller as a fraction of full scale. So even with higher supply voltage for the power stage PV_{DD}, the same THD+N shape with shifted power axis is expected.

The THD+N versus input frequency is shown in Fig. 19.3.4. The plot shows less than 0.006% THD+N for most frequencies and output powers. Even at the worst peak, which is for a non-clipped full-scale output and a high frequency input, less than 0.012% THD+N is achieved.

Figure 19.3.5 shows the output spectrum with 10W output power into a 4Ω load. The THD+N for this case is 0.0018%. The 2nd-order distortion limits the THD+N and mainly comes from the signal DAC in the controller.

A summary of the measured results for the controller with PV_{DD} = 35V is shown in Fig. 19.3.6. The micrograph of the controller is shown in Fig. 19.3.7. The chip size is 4.8mm×4.8mm. The chip uses a 5V supply for the analog circuits and a 1.8V supply for the digital section. The chip has 2 channels for stereo.

References:

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[3] E. Gaalaas, B. Y. Liu and N. Nishimura, "Integrated Stereo Delta-Sigma Class D Amplifier," *IEEE ISSCC Dig. Tech. Papers*, pp. 120-121, Feb., 2005.
[4] K. Philips, J. van den Homberg and C. Dijikmans, "PowerDAC: A Single-Chip Audio DAC with a 70%-Efficient Power Stage in 0.5um CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 174-175, Feb., 1999.
[5] L. Risbo, "Discrete-Time Modeling of Continuous-Time PWM Loops," *AES 27th Int'l. Conference on Efficient Power Amplifiers*, Sept., 2005.

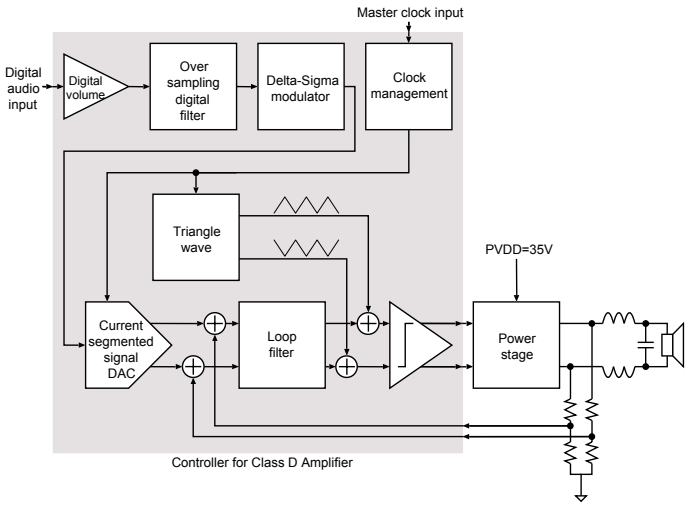

Figure 19.3.1: Controller block diagram.

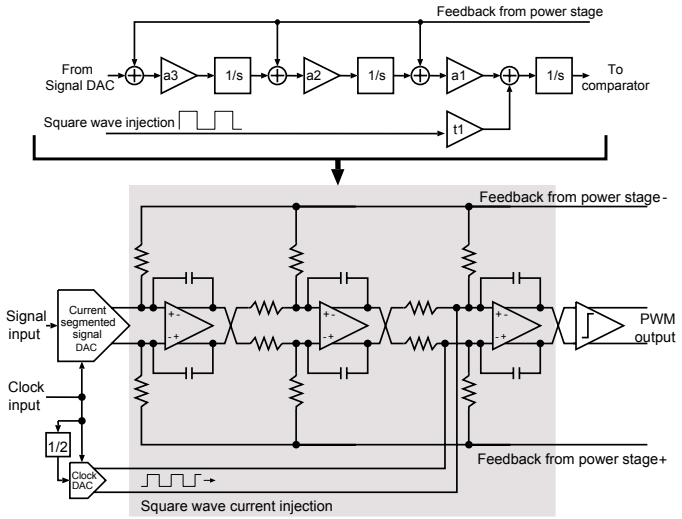

Figure 19.3.2: Loop filter for the pulse-width modulator.

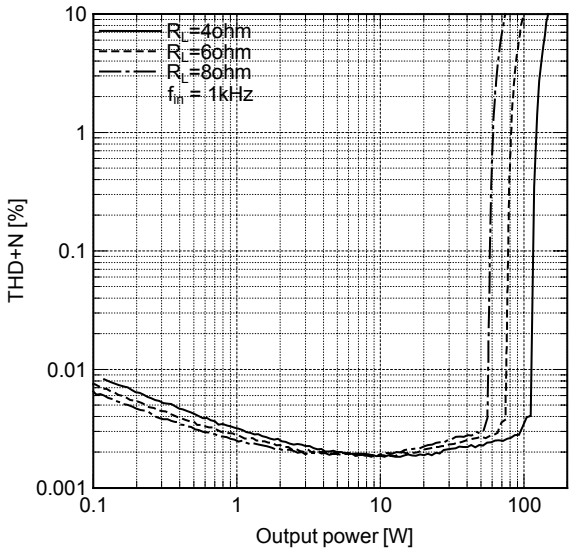

Figure 19.3.3: THD+N versus output power.

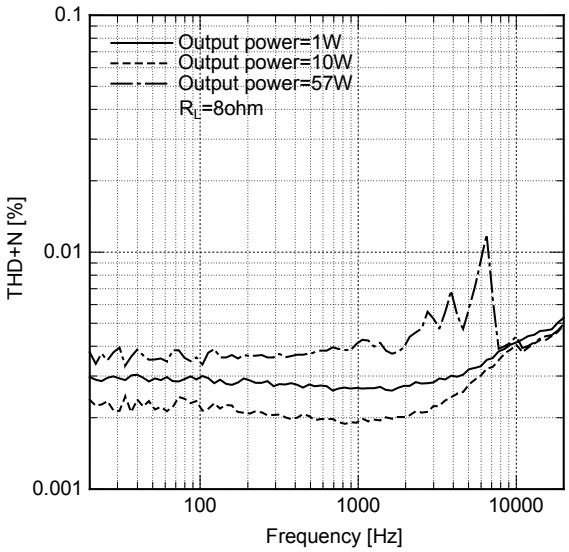

Figure 19.3.4: THD+N versus input frequency.

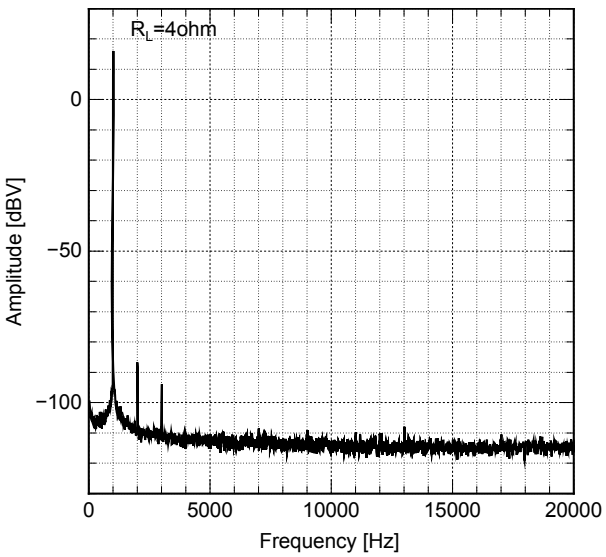

Figure 19.3.5: Output spectrum with 10W output power into 4Ω load.

Power supply	PV_{DD}	35V
	Controller (analog supply)	5V
	Controller (digital supply)	1.8V
Output power	R_L = 4ohm, 10% THD	2 x 130W
	R_L = 6ohm, 10% THD	2 x 99W
	R_L = 8ohm, 10% THD	2 x 74W
THD+N	R_L = 4ohm, P_{OUT} = 100W	0.004%
	R_L = 4ohm, P_{OUT} = 10W	0.0018%
	R_L = 4ohm, P_{OUT} = 1W	0.0032%
Dynamic range	A-Weighted	113dB
Channel separation	57W power into 8 ohm at other channel	109dB
Efficiency	2 x 100W into 4 ohm	81%
Switching frequency	F_s = 32, 48, 96, 192kHz	768kHz
	F_s = 44.1, 88.2kHz	705.6kHz
Die size (stereo controller)	4.8mm x 4.8mm	= 23.04mm^2

Figure 19.3.6: Performance summary.

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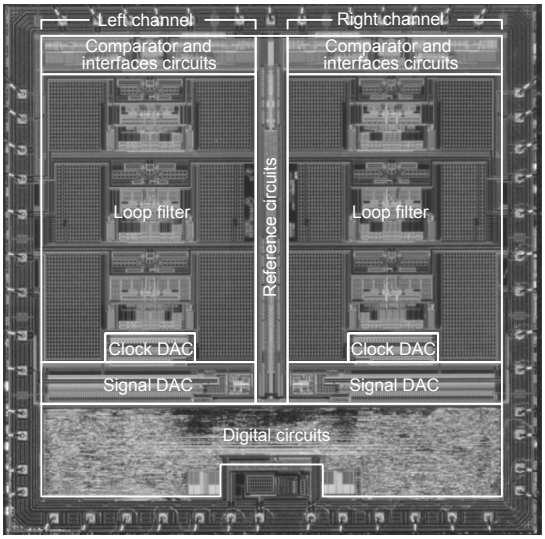

Figure 19.3.7: Chip micrograph.

